Amendments to the Claims:

This listing of claims replaces all prior versions, and listing, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus for allocating one or more resources within a microprocessor to a decoded instruction, the apparatus comprising:

a sequence generator within the microprocessor that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the resources within the microprocessor; and

a resource identifier selector within the microprocessor coupled to the sequence generator, the resource identifier selector determining how many of the resource identifiers, if any, are required by the decoded instruction and selecting one or more of the resource identifiers for allocation to the decoded instruction, and whenever the one or more resources are not allocatable, generating a decoder stall signal.

Claim 2 (previously presented): The apparatus as recited in claim 1, wherein the resource identifier selector determines how many of the resource identifiers, if any, are required by the decoded instruction based on an instruction requirements signal received from an instruction decode unit.

Claim 3 (previously presented): The apparatus as recited in claim 1, further comprising a buffer including two or more buffer entries wherein each resource within the microprocessor comprises one of the buffer entries.

Claim 4 (previously presented): The apparatus as recited in claim 3, wherein the buffer comprises a reorder buffer, a load buffer or a store buffer.

Claim 5 (previously presented): The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a selector coupled to the one or more comparators and the resource identifier selector.

Claim 6 (previously presented): The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a variable shifter coupled to the one or more comparators and the resource identifier selector.

Claim 7 (previously presented): The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison;

a selector coupled to the one or more comparators and the resource identifier selector; and

a highest identifier allocation circuit coupled to the selector.

Claim 8 (original): The apparatus as recited in claim 1, wherein the sequence generator further comprises:

a logic circuit coupled to the resource identifier selector; and

a storage array coupled to the logic circuit and the resource identifier selector.

Claim 9 (original): The apparatus as recited in claim 1, wherein the sequence generator further comprises a storage array coupled to the resource identifier selector.

Claim 10 (original): The apparatus as recited in claim 1, wherein the sequence generator further comprises a logic circuit coupled to the resource identifier selector.

Claim 11 (canceled)

Claim 12 (original): The apparatus as recited in claim 1, wherein the portion of a pseudorandom sequence comprises a first resource identifier from within the pseudorandom sequence.

Claim 13 (previously presented): The apparatus as recited in claim 12, wherein the resource identifier selector comprises means for generating a second resource identifier from within the pseudorandom sequence based upon the first resource identifier.

Claim 14 (previously presented): The apparatus as recited in claim 1, wherein the sequence generator comprises a storage array and the portion of the pseudorandom sequence comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within the storage array.

Claim 15 (original): The apparatus as recited in claim 14, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

Claim 16 (previously presented): The apparatus as recited in claim 14, wherein the resource identifier selector comprises a variable shifter configured to shift elements of the storage array and the resource identifier selector is configured to index the elements within the storage array.

Claim 17 (previously presented): The apparatus as recited in claim 1, wherein the sequence generator comprises a logic circuit and the portion of a pseudorandom sequence

comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within the storage array.

Claim 18 (original): The apparatus as recited in claim 17, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

Claim 19 (previously presented): The apparatus as recited in claim 17, wherein the resource identifier selector comprises a selector and a circuit to determine the highest identifier allocated configured to shift elements of the storage array and the resource identifier selector is configured to index the elements within the storage array.

Claim 20 (currently amended): A method for allocating one or more resources within a microprocessor to a decoded instruction, the method comprising the steps of:

generating one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the resources within the microprocessor;

determining how many of the resource identifiers, if any, are required by the decoded instruction; ~~and~~

selecting one or more of the resource identifiers for allocation to the decoded instruction; and

generating an instruction decode stall signal in response to a determination that the resource within the microprocessor corresponding to the selected resource identifier is not allocatable.

Claim 21 (previously presented): The method as recited in claim 20, wherein the step of determining how many resource identifiers, if any, are required by the decoded instruction is based on an instruction requirements signal received from an instruction decode unit.

Claim 22 (original): The method as recited in claim 20, further comprising the step of comparing a selected resource identifier to an allocation bound and issuing a control signal in response to the comparison.

Claim 23 (original): The method recited in claim 20, wherein the portion of the pseudorandom sequence comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within a storage array.

Claim 24 (original): The method as recited in claim 23, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

Claim 25 (original): The method as recited in claim 20, further comprising:

storing the portion of the pseudorandom sequence as elements within a storage array; and

the selecting step comprises the steps of shifting the elements of the storage array and indexing the elements of the storage array in response to the shifting.

Claim 26 (original): The method as recited in claim 20, wherein the selecting step comprises the steps of:

identifying a most recently associated resource identifier from within the pseudorandom sequence; and

selecting a resource identifier from within the pseudorandom sequence based upon the most recently associated resource identifier.

Claim 27 (previously presented): The method as recited in claim 20, wherein the selecting step comprises the steps of:

determining a requirement of the decoded instruction for a resource within the microprocessor; and

associating the selected resource identifier with the decoded instruction in response to the determination.

Claim 28 (previously presented): The method as recited in claim 20, wherein the selecting step comprises the steps of:

comparing the selected resource identifier to an allocation bound to determine whether a resource within the microprocessor corresponding to the selected resource identifier is allocatable; and

associating the selected resource identifier with the decoded instruction in response to the determination.

Claim 29 (previously presented): The method as recited in claim 28, further comprising the step of modifying the allocation bound in response to a deallocation of a resource within the microprocessor.

Claim 30 (canceled)

Claim 31 (currently amended): A system comprising:

a memory storage device;

a bus coupled to the memory storage device;

a microprocessor coupled to the bus, comprising a resource allocator for allocating one or more resources within the microprocessor to a decoded instruction; and

the resource allocator comprising:

a sequence generator that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the resources within the microprocessor; and

a resource identifier selector coupled to the sequence generator, the resource identifier selector determining how many of the resource identifiers, if any, are required by the decoded instruction and selecting one or more of the resource identifiers for allocation to the decoded instruction, and whenever the one or more resources are not allocatable to the decoded instruction, generating a decoder stall signal.

Claim 32 (previously presented): The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a selector coupled to the one or more comparators and the resource identifier selector.

Claim 33 (previously presented): The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a variable shifter coupled to the one or more comparators and the resource identifier selector.

Claim 34 (previously presented): The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selector and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison;

a selector coupled to the one or more comparators and the resource identifier selector; and

a highest identifier allocation circuit coupled to the selector.

Claim 35 (original): The system as recited in claim 31, wherein the sequence generator further comprises:

a logic circuit coupled to the resource identifier selector; and

a storage array coupled to the logic circuit and the resource identifier selector.

Claim 36 (original): The system as recited in claim 31, wherein the sequence generator further comprises a storage array coupled to the resource identifier selector.

Claim 37 (original): The system as recited in claim 31, wherein the sequence generator further comprises a logic circuit coupled to the resource identifier selector.

Claim 38 (currently amended): An apparatus for allocating one or more resources within the execution path of a microprocessor to a decoded instruction, the apparatus comprising:

a sequence generator within the microprocessor that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the resources within the execution path of the microprocessor; and

a resource identifier selector within the microprocessor coupled to the sequence generator, the resource identifier selector determining how many of the resource identifiers, if any, are required by the decoded instruction and selecting one or more of the resource identifiers for allocation to the decoded instruction, and whenever the one or more resources are not allocatable to the decoded instruction, generating a decoder stall signal.

Claim 39 (new): The apparatus as recited in claim 1, wherein the one or more resources comprise one or more reorder buffer entries.

Claim 40 (new): The method as recited in claim 20, wherein the one or more resources comprise one or more reorder buffer entries.

Claim 41 (new): The system as recited in claim 31, wherein the one or more resources comprise one or more reorder buffer entries.

Claim 42 (new): The apparatus as recited in claim 38, wherein the one or more resources comprise one or more reorder buffer entries.